

Designing industrial pump and fan applications with Altera FPGA and Alizem Motor-Control IP

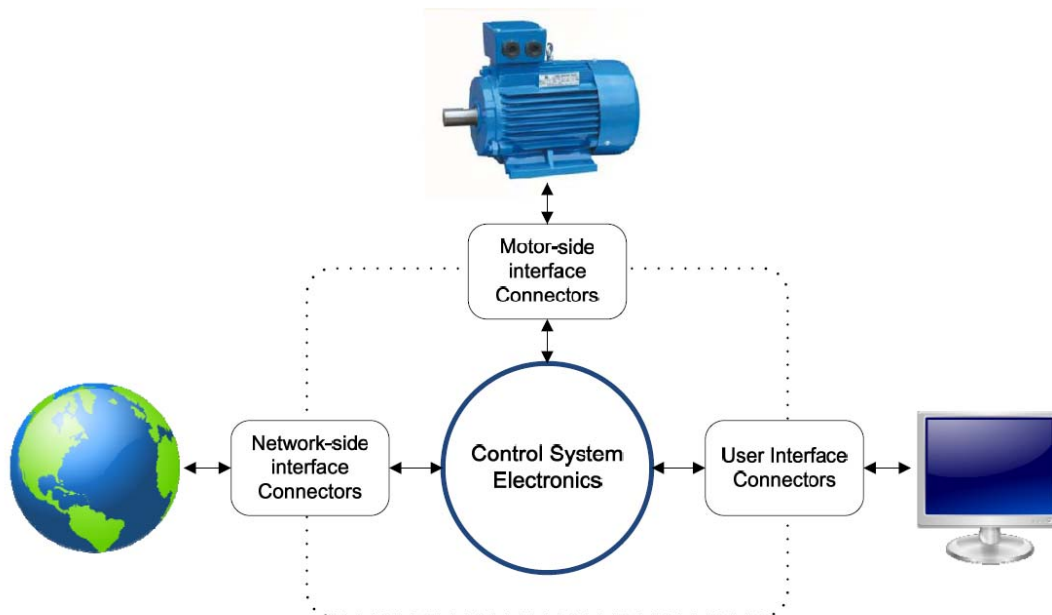
Introduction

Pumps and fans are prevalent within the industrial sector. Chemical, paper, refineries, and water treatment facilities to name a few consume about 40% of their energy driving devices of this type [1]. Hence, pump and fan management represents a key focus area to attain significant energy savings. The most popular approach to saving energy in these applications is to implement adjustable-speed motor drive (ASD) systems, also known as variable-frequency motor drive systems (VFD). Several studies report that the use of ASD systems can reduce total power consumption by 20% to 50% in typical industrial pump and fan applications.

A typical ASD system is composed of three main components: (1) an electric motor, (2) a power converter and (3) a control system. The electric motor drives the load (fan or pump) and is powered via the power converter. The power converter controls the motor speed and hence the power delivered to the motor, by appropriately sequencing power devices within this converter that are connected to each motor phase. This speed adjustment is critically important since in applications of this type, the energy consumed increases in proportion to the cube of the motor speed - therefore operating the fan or pump at the lowest possible speed to meet the application needs results in significant energy savings.

The heart of any control system is the chip on which the control software runs. This white paper outlines how Altera’s Field-Programmable Gate Array (FPGA) chip and Alizem’s Motor Control Intellectual Property (IP) core technologies are of benefit to the design of industrial ASD’s for pump and fan applications in terms of increased performance, cost reductions and time-to-market.

Figure 1 - Typical Motor Control System



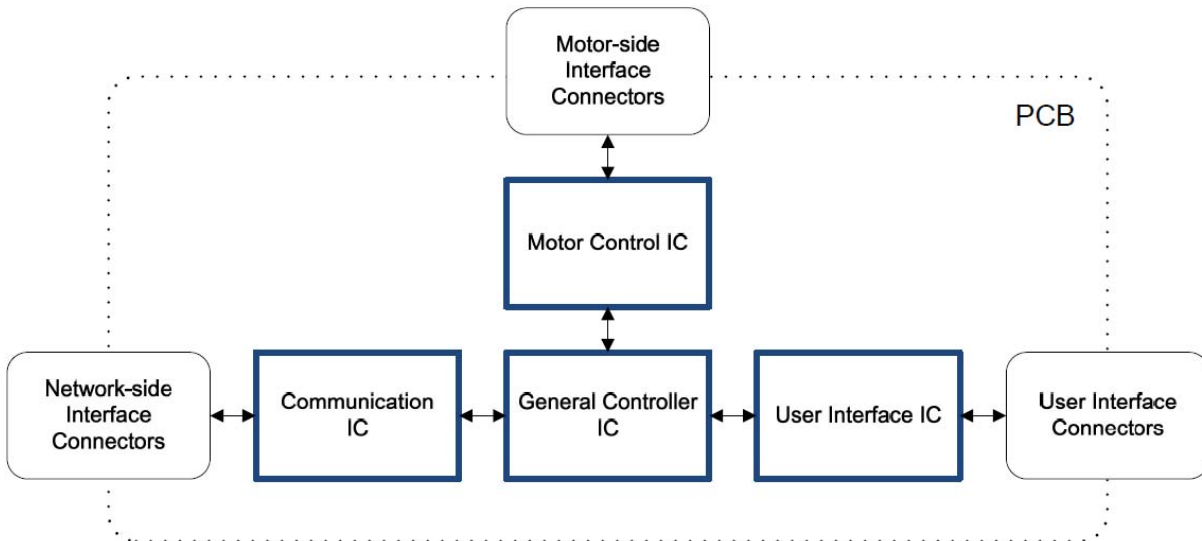
Conventional vs. FPGA-based Motor Control System Design

A typical motor control system is composed of four main sub-systems as shown in Fig.1: (1) a motor interface which includes the PWM power converter and relevant current, speed, and position transducers, (2) a networked/remote communication interface, (3) a local interface that allows users to monitor the system on-site via hand held or laptop units and, (4) a core electronic system that binds those sub-systems together to allow their proper interaction with each other. The difference between a conventional and a FPGA-based motor control system design lies in how the control electronic system is designed.

Conventional approach

The conventional motor control system illustrated in Fig. 2 implements the motor control system using a segmented architecture. A general purpose controller chip - typically an MCU - interfaces to a networking/ communication IC (a suitable hardware interface chip for local communications) and a dedicated motor control IC (motor control MCU or DSP). Specific sensor information generally feeds into the motor control IC portion of this implementation via some dedicated hardware circuitry. Managing the proper operation and hardware linkages among these dedicated IC's is an integral part of the challenge faced by designers of conventional systems of this type.

Figure 2 – Control System Electronics design with PCB-integrated components



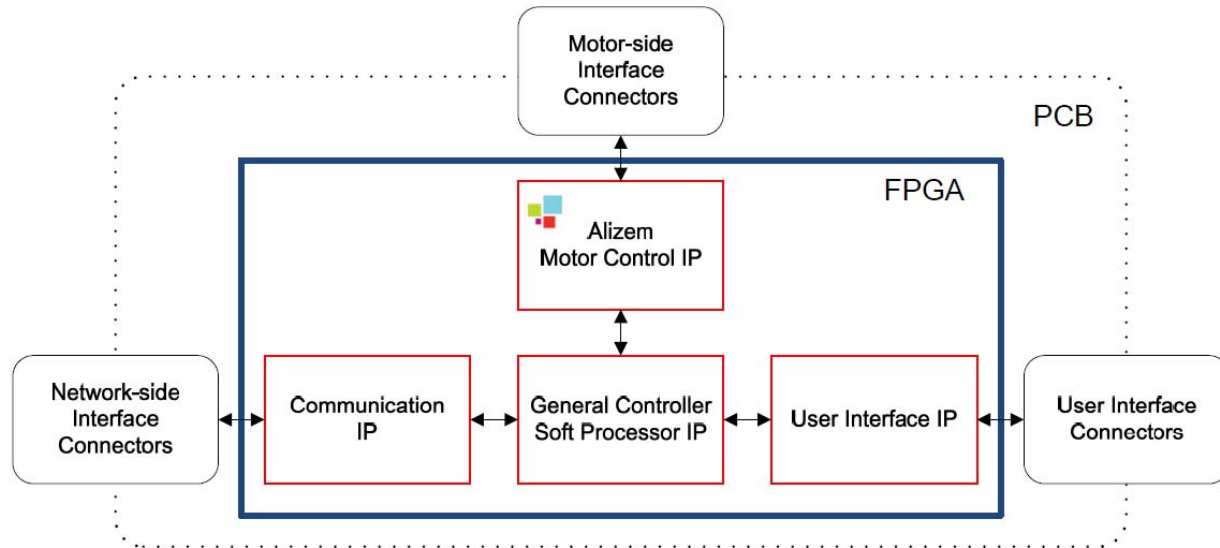
Although in the early 90's this approach revolutionized motor control system design, it has some fundamental limitations in terms of integration, reliability and flexibility. The physical PCB integration of numerous components requires substantial design time and effort, and drives the need to perform extensive electrical and reliability testing before launching a production ready product. The ultimate reliability of the design is negatively affected by the number of discrete parts used in this design approach both from a manufacturing and component level perspective. Designs of this type do not offer much flexibility, if any, in terms system performance/feature upgrades and can require significant engineering effort and re-design should there be a need to substitute key components with alternate devices.

More specifically, Motor Control IC's are driven by a one-fits-all design mentality that drives volumes and ROI for the supplier. As such, they tend to restrain system flexibility that may be key to securing the most energy savings benefits for your specific application. Those limitations have an impact on system development costs where the gap between the Motor Control IC set of features and applications requirements must be worked out by the system designer.

System-on-a-programmable-chip FPGA-based approach

The FPGA-based approach has the exact same system architecture as the conventional approach except that the segmented functions described in the conventional implementation are now fully integrated into a single FPGA component. The FPGA is loaded with optimized custom software/IP components tailored specifically for the application at hand as shown in Fig. 3.

Figure 3 – Control System Electronics design with FPGA-integrated components



This decoupling of hardware and functionality provides a superior level of integration that translates into many well-known benefits for the system designer such as: increased design flexibility and speed, reduced component integration challenges, lower risk of component obsolescence, and lower total cost of ownership (TCO) [2,3]. Here is how value is provided to FPGA-based motor control system designers:

- **Flexibility of design:** the Motor Control IP can be tailored to designer’s specific application needs without having to modify or add any hardware components. This also means that design modifications can be made very late in the design cycle or even in the field once the system has been released or is undergoing field trials (Field-Programmable).
- **Increased speed and ease of component integration:** Available FPGA IP components can be added or removed from the design within seconds through software re-programming of this versatile component. This device programmability allows designers to accelerate their design iterations within a single design environment compared to the time required by conventional design processes relying on discrete components. Hence, more time is available to focus on product differentiation and system performance testing. For motor control, this adds an opportunity to invest more time and effort to develop system diagnostics and bi-directional communications between the general controller and the Motor Control IP.
- **No chip obsolescence & option to benefit from new semiconductor process technologies:** The same control system can easily be ported to a different family of Altera® FPGAs should there be a need to take advantage of next generation IC footprint advantages, cost, or performance aspects.
- **Lower total cost of ownership:** FPGA-based control systems allow “single chip” solutions which greatly simplify the manufacturing complexity of the product and the supply chain logistics of your design. These benefits translate to lower product costs and reduced risk of supply chain issues. The ability to program these systems in the field enables the base design to be enhanced with new and improved features that can be added over time. This can be leveraged to provide a source of after-market revenues. Such an opportunity is not generally possible in a conventional discrete IC based design implementation.

Alizem Pump and Fan Motor-Control IP value-added features

Based on the FPGA-based motor control system design approach above, Alizem's Motor control IP provides the system designer with an off-the-shelf Motor Control IC in a software (IP) form factor designed for integration directly onto an FPGA device. It offers the same conventional features of Motor Control IC's such as PWM and speed regulation plus new value-added features that are enabled by the FPGA/IP combination as outlined below [6]:

- **On-line power consumption estimator feature** that provides information regarding the motor's instant power consumption or amount of total energy consumed by the controller. This information may then be used to monitor and control the energy consumption of the system and contribute to the optimal energy management of the system. This feature can be integrated into a smart-meter /smart-grid master applications.
- **Power converter test and debug features** that can be used by the system developer to quickly and easily test the proper operation of the power converter prior to its integration with the real motor. Rather than developing their own test module, the motor control system designers can use Alizem's Motor Control IP in debug mode to test their power converter stage operation before connecting to a real motor, enabling them to save design time.
- **Customizable pin layout:** By using the pin assignment flexibility inherent in an FPGA design versus the fixed constraints presented by discrete IC's, the PCB layout can be optimized to minimize its size and to optimize critical signal paths.
- **On-line virtual motor simulator** features emulate motor operation on the FPGA providing the software developer with a system to test their application on before initiating hardware integration with a real motor.
- **Control multiple motors in parallel:** multiple instances of Alizem's Motor Control IP can be housed and programmed on the same FPGA chip and controlled independently using the same software drivers. This feature is useful when one wishes to synchronize the startup of multiple motors or to minimize total peak in-rush line currents (smart-grid consideration).
- **No VHDL to learn or complex motor drivers to develop:** The software API is easy for non motor-control or FPGA experts to use as a system design tool.

Motor control scheme and typical applications

Alizem Motor Control IP for Pump and Fan Applications is based on a V/Hz or scalar control motor scheme. This AC motor control approach is ideal for applications that have predictable and well behaved dynamics load and speed requirements such as those found in fan and pump type loads [4]. A typical application example is a system where solar energy is hydraulically stored using a water pump [5].

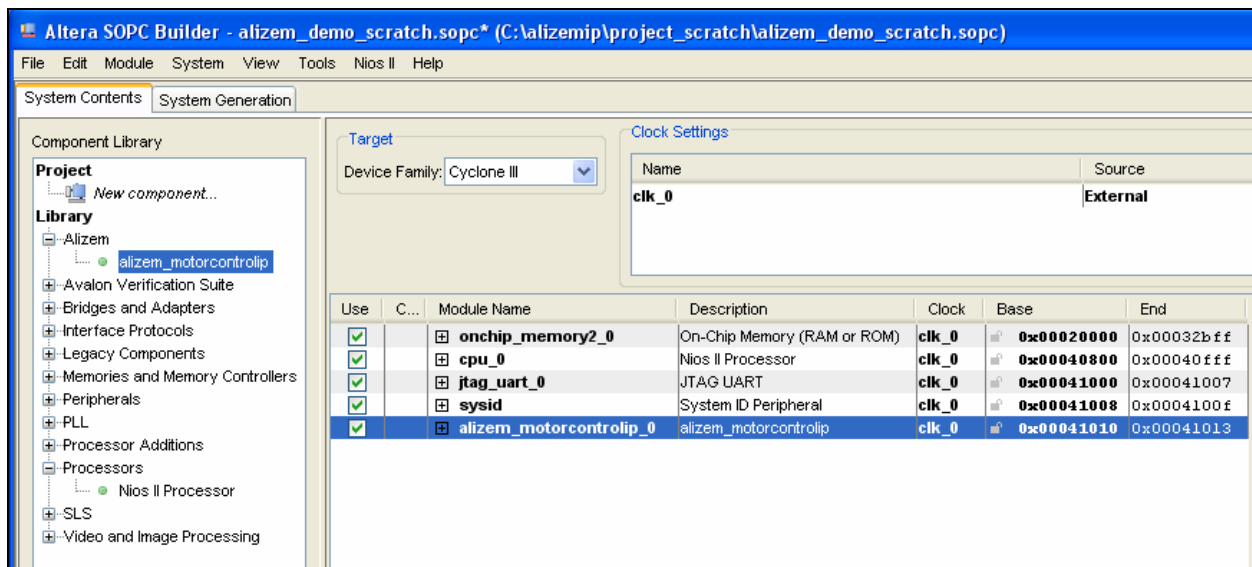
Integrating Alizem's Motor Control IP in a FPGA-based Motor Control systems using Altera's EDA tools in less than 30 minutes

The process of designing an FPGA-based motor control system using Altera's device and EDA tools and Alizem's Motor Control IP is partitioned into three steps: (1) selection of system components, (2) assign system connection to external pins and hardware system generation, (3) application software development.

Selecting system components using Altera's System-On-a-Programmable-Chip (SOPC) Builder

The SOPC Builder tool is part of the Quartus[®] II design environment. Its purpose is to quickly build and generate a system around a Nios[®] II processor using the Avalon[®] switch fabric technology. For example, in a simple motor control design, you may integrate a Nios II processor component, a memory component and Alizem's Motor Control IP component (Figure 4). The components may come from Altera or from 3rd-party IP providers such as Alizem.

Figure 4 – SOPC Builder component configuration example with Alizem's Motor Control IP



Once your system is properly configured, connection between components is done automatically by the SOPC Builder software. The resulting system output is integrated directly into your Quartus II design.

System connection to external pins and hardware system generation

The next step is to link your SOPC system to external FPGA pins. This pin assignment is driven by layout constraints with the rest of the system (i.e. power converter, LCD screen, buttons, etc.). You may also insert components between the SOPC system and the external pins to support signal conditioning requirements needed for your application.

Once this is done, system generation (synthesis and fitting on the FPGA device resources) is done automatically by the Quartus II design tool. The resulting output is the hardware part of the FPGA system and may be used to design and debug software applications running on the Nios II soft processor.

Application software development

Software development for Altera's FPGA-based project is done using the Nios II Embedded Design Suite (EDS). This suite features a complete set of software development tools that runs inside the popular Eclipse environment. This software development environment is designed so that you can have the same application software running on different sets of FPGA hardware configuration and device drivers (often called a Board Support Package or BSP). The BSP is generated automatically by the Nios II tools from the system generated inside Quartus II at the preceding step. You may then build you application on top of this BSP using Alizem's Motor Control IP drivers.

Here's a short code example in which one motor instance is declared, dead-time of the power converter is set to 4us (given that system clock is running 50 MHz), ramp speed acceleration is set to 100 rpm per second, motor speed is set to 25% of nominal speed, load factor is set to 0.5 p.u., "run" operation mode is selected and estimated speed and power consumption are printed every second (refer to datasheet for more technical details [7]) :

```
extern alizem_motorcontrolip motor1;

int main {

    set_nominal_parameters(motor1, 500, 6000, 91) ; 500W Motor, 6000 RPM, 0.91 Nm Torque

    set_deadtime(motor1, 100);                ; 100x50e-6 = 2µs
    set_speed_ramp(motor1, 100);              ; 100 RPM per second
    set_load_type(motor1, 2);                 ; centrifugal pump
    set_mode(motor1, 1);
    set_speed(motor1, 16);                    ; 16/256*6000 = 375 RPM = 0.0625 p.u.

    while(1){
        printf("Motor1 estimated speed (rpm): %d ", get_speed(motor1))
        printf("Motor1 estimated power consumption (W): %d\n", get_powerest(motor1));
        usleep(1000000);
    };

    return 0;
}
```

Here's the output for five seconds :

```
Motor1 estimated speed (rpm): 0 Motor1 estimated power consumption (W): 0
Motor1 estimated speed (rpm): 100 Motor1 estimated power consumption (W): 1.67
Motor1 estimated speed (rpm): 200 Motor1 estimated power consumption (W): 13.32
Motor1 estimated speed (rpm): 300 Motor1 estimated power consumption (W): 44.96
Motor1 estimated speed (rpm): 375 Motor1 estimated power consumption (W): 87,81
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```

Conclusion

Designing motor control systems for industrial pump and fan applications using Altera's FPGA and Alizem's Motor IP is a compelling alternative over conventional approaches. This design approach offers performance, reliability, costs and time-to-market benefits to name a few. The table below compares conventional COTS Motor Control IC and COTS Alizem Motor Control IP:

| | Conventional Motor Control IC | Alizem Motor Control IP |
|------------------------------------|---|--------------------------------------|
| Form factor | Discrete component (real chip) | Software/IP component (virtual chip) |
| Quality | May vary | Constant |
| Supply | May be limited | Unlimited |
| Lead time | Weeks-months | None |
| Evolve over time | No | Yes |
| Chip obsolescence | May happen. | No. |
| Motor control application-specific | No – generic | Yes – specific |
| Integration with main controller | Tedious | Automatic |
| Software drivers | Must be developed on main controller by design team | Included. |
| Pin layout | Fixed | Customizable |

Tight integration between Alizem Motor Control IP and the Nios II processor makes it an ideal solution for any smart-grid applications where the basic principle is to share information between energy generation points and energy consumption points. Information made available by Alizem Motor Control IP can then be easily processed on the Nios II processor and transmitted through industrial communication IP such as Industrial Ethernet protocols or fieldbusses.

The software form factor and evolving capability of Alizem Motor Control IP makes it an excellent choice for designers who are seeking a way that permits to leverage their own product differentiation while at the same time reduce development costs and time-to-market.

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