

## General Description



This document presents detailed technical information regarding Alizem Motor Control IP Core for Pump and Fan applications. The Alizem Motor Control IP Core is intended to be integrated into Altera® FPGA-based low-voltage motor drive systems. Its design is based on a V/Hz (or scalar) motor control method with space vector PWM (SVPWM) and it can be used with either open-loop or closed-loop speed control.

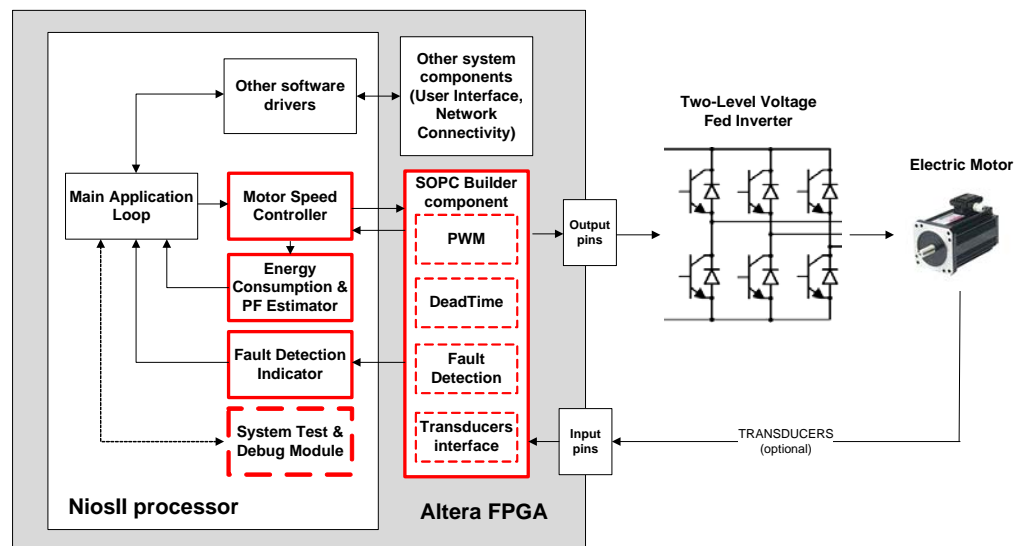
### Features

- ✓ Designed for Permanent Magnet Synchronous (with sinusoidal back-emf and trapezoidal back-emf BLDC) and Induction Motors
- ✓ Optimized V/Hz for maximum energy efficiency
- ✓ Smart-grid ready with integrated energy consumption estimation
- ✓ Safety operation with fault detection capability
- ✓ Configurable dead-time for minimized harmonic losses and noise
- ✓ Fixed or variable speed operation
- ✓ SOPC Builder-ready component for Altera FPGAs
- ✓ Hardware and software optimized for small FPGA footprint
- ✓ Quick and easy-to-integrate: No extensive FPGA or Motor Control skills required
- ✓ IP Core form factor: guarantees perfect quality, eliminates inventory and lead time
- ✓ Early SW development with System & debug Module virtual motor

### Typical Applications and Markets

- ✓ Pump and fan applications
- ✓ HVAC
- ✓ Any Low Dynamics applications
- ✓ Consumer, Industrial, Automotive, Defense markets

### Typical System Schematic



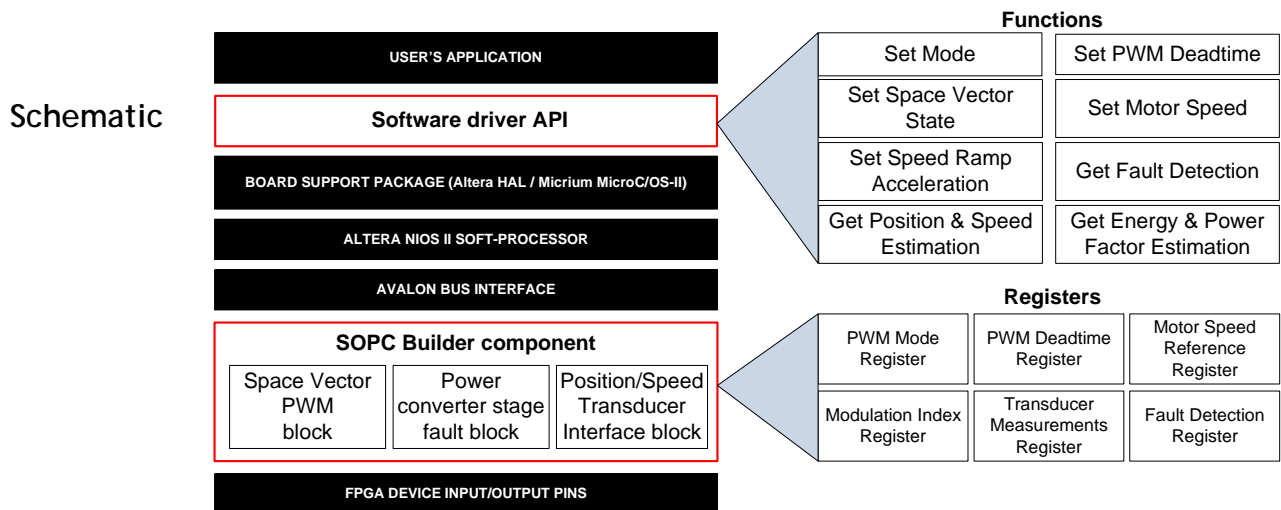
### Deliverables

- ✓ Encrypted SOPC Builder component + License
- ✓ Application Programming Interface (API) software library for Nios® II processors
- ✓ Easy-to-understand User Manual & Reference design
- ✓ Full integration support (internet / phone / onsite) & IP customization engineering
- ✓ Free IP demo available to be used on Altera development board

## Architecture description

The Motor Control IP Core is composed of two main components:

- ✓ A *System-on-a-Programmable-Chip (SOPC) Builder* component: control register interface, Space Vector Pulse Width Modulation (PWM) block, power converter stage fault block and optional position/speed Transducer Interface block.
- ✓ A Nios II software layer (API) that includes the following commands: a mode selector, a motor speed controller, an energy consumption estimator, a power factor estimator, a fault detection indicator and a system test & debug module.



### *Set Operating Mode*

This function sets the IP in either (1) debug mode or (2) run mode.

### *Set PWM Deadtime*

This function sets the correct PWM deadtime for avoid shoot through faults and minimize noise and voltage time-harmonics.

### *Set Space Vector State* (debug mode only)

## Software driver API

This function manually sets the power converter state according to one space vector state (SV0-7) and to check voltage correspondence on phase lines during system debug process.

### *Set Motor Speed*

This function sets the desired steady-state mechanical speed of the motor.

### *Set Speed Ramp Acceleration*

This function sets the desired ramp acceleration during transient state.

*Get Fault Detection*

This function flags any fault detected on the power converter stage side.

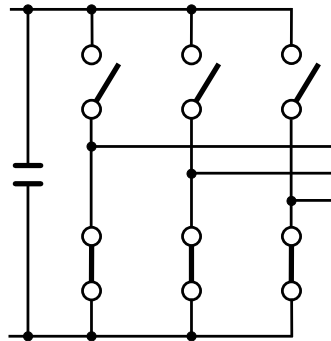
*Get position and speed estimation (virtual motor)*

This function estimates the motor shaft mechanical speed and position while the motor is running. This function also allows early application software development before the actual system is ready to operate.

*Get Energy and Power Factor Estimation*

This function estimates the motor power consumption and its total energy consumption during a period of time based on load torque profile and motor speed.

This IP has 6 PWM output pins connected to the 3 arms of the 2-level inverter input pins. The state of each pin for the 8 space vector states are described below (0 = IGBT is not conducting, 1 = IGBT is conducting).



SOPC  
Builder  
component  
Output pins

SV State	PWM1	PWM2	PWM3	PWM4	PWM5	PWM6
0	0	1	0	1	0	1
1	1	0	0	1	0	1
2	1	0	1	0	0	1
3	0	1	1	0	0	1
4	0	1	1	0	1	0
5	0	1	0	1	1	0
6	1	0	0	1	1	0
7	1	0	1	0	1	0

SOPC  
Builder  
Component  
input pins

*Power converter stage fault pin*

Connect your power module output fault pin to this pin to turn off PWM within one clock cycle and send a signal to the controller.

*Speed transducer pins*

Connect your motor's shaft speed transducer output pins to those pins to provide information to the controller and to enable closed-loop speed control.



**Motor Control IP Core  
for Pump and Fan Applications  
Datasheet for Altera FPGAs**

	Parameter	Default	Range	Unit	Details / Description
<b>System Parameters</b>	Motor Type	0	0-2	-	0 = PMSM, 1 = BLDC, 2 = IM
	Motor Number of Pair of Poles	2	1-3	Pair(s) of Poles	To set synchronous speed
	Load Type	0	0-2	-	0 = Constant (positive displacement), 1 = Linear, 2 = Squared (centrifugal)
	Torque constant	0	0-255	-	Depends on load type
	Speed Control loop Frequency	1000	100-5000	Hz	Depends on load inertia
	PWM Switching Frequency	4	1-25	kHz	Switching frequency of the PWM
	System Clock Frequency	50	$1 < f < f_{max}$	MHz	Operating clock frequency of the IP
	Dead-time	200	1-255	Clock cycle	Dead-time of the PWM based on System Clock cycle units. Ex. $200 \times 20ns = 4 \mu s$

### Integration Quick Steps

This Motor Control IP is designed to be integrated in your system in less than 30 minutes by following these steps:

- (1) SOPC Builder component integration,
- (2) System connection to external pins and hardware system generation,
- (3) Application software development using built-in software drivers.

### Resources Utilization and Performance

**Altera Cyclone® III/IV FPGAs**

Tested on an EP3C40F484C7N Altera FPGA device controlling a 500W Danaher Motion PMSM motor powered by a Fairchild FSBB15CH60C Smart Power Module (EBV's Falcon Eye Motor Control platform). Logic Elements (LEs) : 400 (approx.) Memory: 720 bits.

Tested on a EP3C40F484C6N Altera FPGA device controlling a 40W Maxon BLDC motor powered by a custom three phases two-level IGBT power stage (Arrow's Motion Fire Control platform). 100 (approx.) Memory: 720 bits.

Designed to fit on Altera Cyclone III/IV (E/GX) FPGAs.



Motor Control IP Core  
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### Special Application Requirements ?

If your application has special requirements to be fit that are not currently included in this Motor Control IP (such as Power Factor Correction, DC Bus Voltage Protection, IEC 61131-3 compatibility, etc.) please contact us and we will be pleased to customize this IP to make it fit perfectly in your application.

### FREE Demo

Contact us for a free time-limited trial demo of this IP. This demo can be integrated into your own system to assess if it meets your needs prior to licensing.

### Three Packaging Options

IP Only	IP is delivered as encrypted software files to be directly integrated on an Altera FPGA inside Altera EDA Tools environment.
Complete SoC	This package consists of a full system - including Alizem Motor Control IP and other IP such as Industrial Ethernet - customized and tested for customer's application. The system is delivered as FPGA configuration files ready to be downloaded to a FPGA chip.
Turnkey solution	This package consists of a complete SoC and all electronics circuits, electrical connectors and mechanical interfaces around it.

### IP Licensing and Price

Please contact Alizem for more information.

## Contact us



For more informations regarding this IP, please contact Alizem Sales department :

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